Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 30 with the following amended paragraph:

These and other drawbacks in the prior art are overcome in large part by a system and method for frame detection and generation according to the present invention. Briefly, each incoming clock-data stream is divided into two independent data streams: a clock path which preserves the timing of the individual [[cock]] clock domains and a data path which multiplexes an arbitrary number of data streams onto a parallel path or bus. A framer [[unit]] state machine is provided to store and update the context of the data streams and to align the data stream to the bus.

Please replace the paragraph beginning at page 2, line 25 with the following amended paragraph:

FIGS. 1-3 illustrate an improved frame detection and generation system. Signal streams are divided into a clock stream and a data stream. Each stream is processed independently. A framer [[unit]] state machine is provided offset the path of the data streams to store and update the context of the data streams and to align the data stream to the bus.

Please replace the paragraph beginning at page 4, line 27 with the following amended paragraph:

The framer state machine 114 calculates the frame position of the new stream in any of a variety of known manners. If the framer [[array]] state machine 114 finds the frame boundary of the data stream and the data stream is not aligned, the framer state machine 114 aligns the time slots of the incoming frames to the 9-bit data bus 136. This is accomplished using the align signal 138, which informs the serial-to-parallel converter 108a, 108b to provide, for example, nine bits during the next data transfer. Thus, time slots of the frame will be aligned in a maximum of seven data transfers as the time slot can be shifted one bit per transfer.

Please replace the paragraph beginning at page 5, line 7 with the following amended paragraph:

During normal operation eight data bits are transported over the 9-bit data bus together with the respective stream identifier. As shown, the data bits transported over the 9-bit data bus 136 during the initial data transfer are misaligned to the incoming frame by one (1) bit. In particular, 210 shows a data transfer where bit 256 of a previous frame and bits 1 through 7 of the actual frame are transported over the 9-bit data bus 136. After the next transfer 212 the framer state machine 114 finds the frame begin. The framer state machine 114 detects the misalignment as described above and then requests a nine bit data transfer via the align signal 214 in order to align the data to the 9-bit data bus 136. 214 shows the following nine bit data transfer which aligns time slot 2 to the internal bus. If the frame and the time slot had been misaligned by more than one (1) bit, the process would repeat until the frame and time slot were aligned, as shown at 216.